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10/813,031	03/31/2004	Hiroki Goko	030712-36	3838

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EXAMINER	
MEMULA, SURESH	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,031	GOKO ET AL.	
	Examiner	Art Unit	
	SURESH MEMULA	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This FINAL office action is a response to the remarks filed on 12/31/2007. The remarks are not persuasive; therefore, the rejections based on the prior art of record, Sano et al., are maintained. Claims 1-5 are pending.

Claim Objections

1. In claim 1, the second step of allocation is synonymous to the well-known placement process involved in realizing a layout design for an IC. Therefore, the second step of allocation is in direct contradiction to Applicant's objected claim limitation "at least the first and second steps are performed **prior to a layout design** of the semiconductor integrated circuit."

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-5 are rejected under 35 U.S.C. 102(e)** as being anticipated by US Pub. No. 2004/0107408 to Sano et al. (Sano).

4. As to Claim 1,

a first step for determining a number of clocks different in delay amount (Paragraphs 0001, 0041, 0051, 0074, 0174; FIG. 5-6, 8-9, 12, 17, 20, 24, 42-45, 49, 51-52), which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof (Paragraphs 0089, 0093; FIG. 2, 16, 22, 36), and determining delays in the clocks on the basis of pre-set conditions for constraints of timings (Paragraphs 0032-0034, 0176; FIG. 2, 21);

a second step for allocating clocks supplied to respective circuits (Paragraphs 0013, 0080, 0160, 0174, 0183, 0191-0192, 0215, 0223, 0231, 0240; FIG. 21); and

a third step for optimizing timings on the basis of a list (Paragraphs 0002, 0062, 0066, 0081, 0158, 0174, 0184; FIG. 2, 21) obtained by the timing constraint conditions (Paragraphs 0032-0034, 0176; FIG. 2, 21) and the clock allocation (Paragraphs 0013, 0080, 0160, 0174, 0183, 0191-0192, 0215, 0223, 0231, 0240; FIG. 21) and determining whether results of analyses of the respective timings correspond to violation of the constraints of timings (Paragraphs 0054-0059, 0179, 0206, 0215), wherein the optimization of the timings is repeated according to the constraint violation of the constraints of timings (Abstract; Paragraphs 0050, 0061, 0065, 0173, 0179, 0182) and

at least the first and second steps are performed prior to a layout design of the semiconductor integrated circuit (FIG. 21).

5. As to Claim 2, a fourth step for generating the clocks different in the delay amount (Paragraphs 0001, 0041, 0051, 0074, 0174; FIG. 5-6, 8-9, 12, 17, 20, 24, 42-45, 49, 51-52) for the verification of a layout design of the semiconductor integrated circuit (Paragraphs 0089, 0093; FIG. 2, 16, 22, 36); a fifth step for adjusting skews for each of said clocks (Abstract; Paragraphs 0002, 0015, 0032);
a sixth step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design (Paragraphs 0001, 0032-0034, 0041, 0051, 0074, 0174; FIG. 5-6, 8-9, 12, 17, 20-21, 24, 42-45, 49, 51-52), respectively; seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design (Paragraphs 0071, 0085, 0089, 0093) and determining whether analytical results of the respective timings correspond to the constraint violation (Paragraphs 0054-0059, 0089, 0093, 0179, 0206, 0215; FIG. 21), wherein the layout adjustment is repeated according to the constraint violation (Abstract; Paragraphs 0050, 0061, 0065, 0173, 0179, 0182; FIG. 21).

6. As to Claim 3, adjusting the delay of each of the clocks again according to the constraint violation when the constraint violation exists in the third step (Paragraphs 0001-0002, 0032-0034, 0041, 0051, 0062, 0066, 0074, 0081, 0158, 0174, 0184; FIG. 5-6, 8-9, 12, 17, 20-21, 24, 42-45, 49, 51-52).

7. As to Claim 4, a step for adjusting delays set for said clocks according to the constraint violation when the constraint violation occurs in the seventh step (Paragraphs 0001-0002, 0032-0034, 0041, 0051, 0062, 0066, 0071, 0074, 0081, 0085, 0089, 0093, 0158, 0174, 0184; FIG. 5-6, 8-9, 12, 17, 20-21, 24, 42-45, 49, 51-52).

8. As to Claim 5, wherein adjusting the delays comprises adding an delay at a starting point where data is outputted (Abstract; Paragraphs 0007, 0050, 0061, 0077, 0173), and determining the clock delays according to the difference between the added value and the cycle of the clock (Paragraphs 0001, 0016, 0041, 0051, 0074, 0174; FIG. 5-6, 8-9, 12, 17, 20, 24, 42-45, 49, 51-52).

Response to Applicant Remarks

8. The applicant states "Sano et al. explicitly discloses an outline of an LSI layout designing method (circuit designing method) that includes simultaneous component layout design (Remarks: page 2, paragraph 3)" and Sano fail to teach "prior to a layout design of the semiconductor integrated circuit (Remarks: page 3, paragraph 1)."

Examiner's response:

9. Applicant's term "a layout design" is interpreted to be a noun; and furthermore, "layout design" is a term of art for a representation of an IC in terms of planar geometric shapes that make up the components of an IC. The term "layout design" is not equivalent to the verb phrase "designing a layout". Therefore, Applicant's claims only necessitate the first and second steps be performed prior to the realization of "a layout design" and not the initiation of the design process itself.

10. Accordingly, in example, Sano creates a clock tree (Paragraph 0041; FIG. 21, element S113) to perform the first step for determining a number of clocks different in delay (Paragraphs 0041, 0051), and subsequently Sano performs the second step for allocating clocks supplied to respective circuits (Paragraph 0080; FIG. 21, element S113). Sano performs the first step (FIG. 21, element S113) and the second step (FIG. 21; S122) prior to realizing a layout design result (FIG. 21, element #20), i.e., prior to a layout design of the semiconductor IC.

11. Furthermore, as is well known in art, the first and second steps directed to timing analysis and allocation, respectively, are commonly performed in preliminary logic design/schematic levels of abstraction; and therefore, the limitation "prior to layout design" is deemed not novel.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

13. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh Memula whose telephone number is (571) 272-8046. The examiner can normally be reached on M-F 8am-4:30pm EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Suresh Memula
Art Unit 2825
March 26, 2008

/Paul Dinh/
Primary Examiner, Art Unit 2825